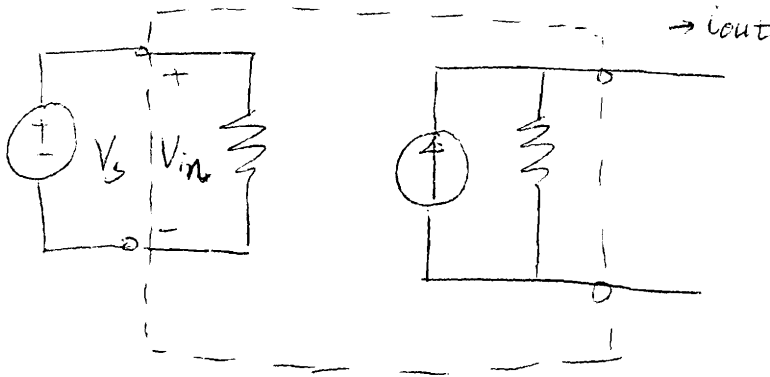


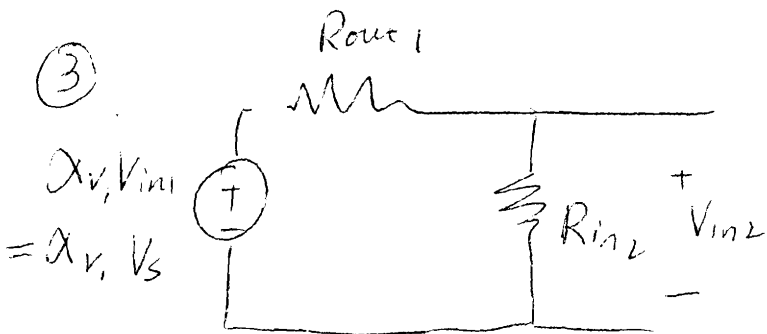
① you can have voltage in, current out



$A_v = G_m R_{out}$ → sign here is determined by logic of the amplifier (inverting, or non-inverting)

$G_m = \frac{i_{out}}{V_{in}} \Big|_{\text{short}}$

② G_m circuit transconductance.
 g_m device transconductance.

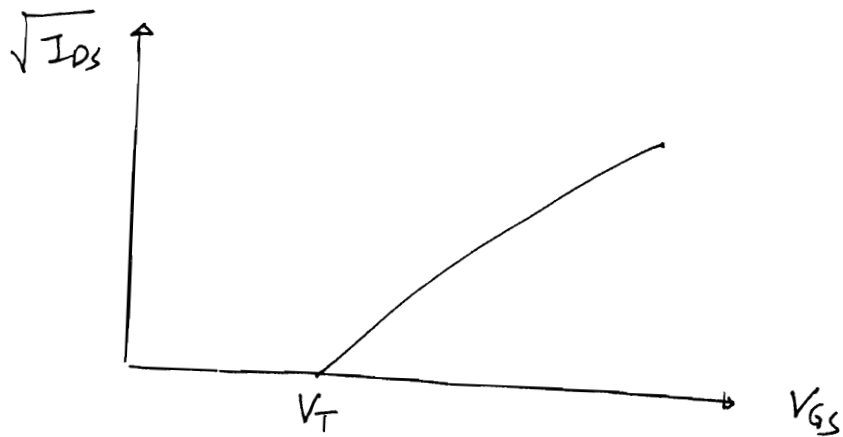


$V_{in2} = \frac{R_{in2}}{R_{out1} + R_{in2}} \cdot \alpha_v \cdot V_{in1}$ Voltage divider!

$V_{out} = \alpha_v \cdot V_{in2} = \alpha_v \cdot \alpha_v \cdot V_{in1} \cdot \frac{R_{in2}}{R_{out1} + R_{in2}}$

you fix V_{DS}

lec#1 SP-2



$$I_{D_S} = \frac{k'}{2} \frac{W}{L} (V_{G_S} - V_T)^2 (1 + \lambda V_{D_S})$$

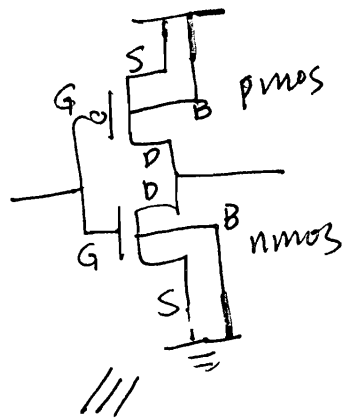
Saying $\lambda \doteq 0$

$$\Rightarrow I_{D_S} = \frac{k'}{2} \frac{W}{L} (V_{G_S} - V_T)^2$$

$$\sqrt{I_{D_S}} = \sqrt{\frac{k'}{2} \frac{W}{L}} (V_{G_S} - V_T)$$

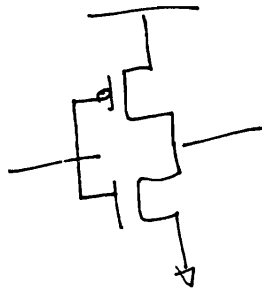
body-effect consider or not?

For digital design:



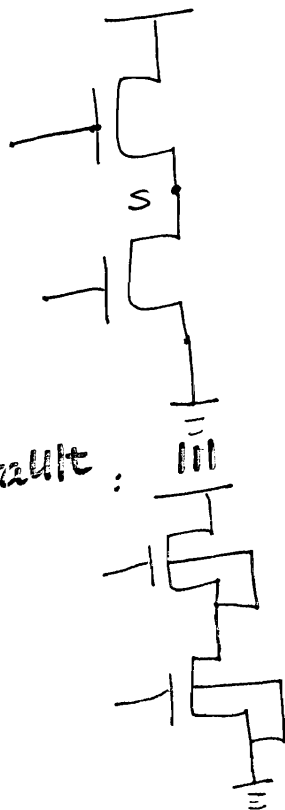
by default.

So if you don't show your Body connection, we assume it is connected to Vdd or ground!

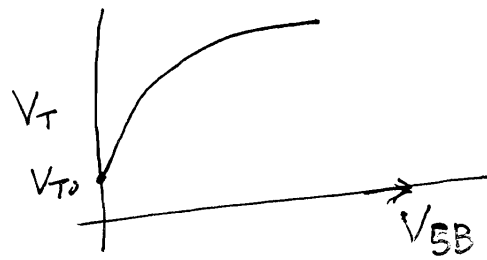


For analog design:

$V_T \uparrow \Rightarrow I_{DS} \downarrow \Rightarrow$ Not working well!



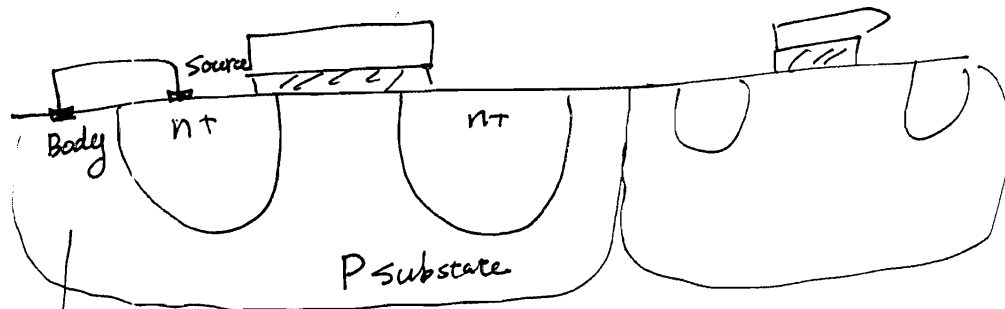
by default:



If $V_{SB} \neq 0$, say V_B is grounded.

we assume $V_{SB} = 0$ by default!!!

In analog design, if you connect source and Body, you are connecting Body to n-well (or P-well)



→ you have to build new wells for other devices. (your source controls body !!)

Can not share wells, otherwise your source will control other devices.

Shortcomings

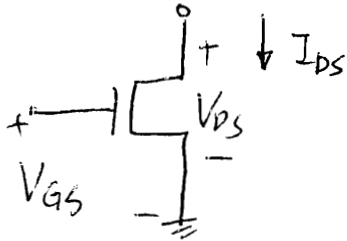
- ① Area consumption !! separate well for every transistor!
- ② Also: if I connect source with Body, parasitic cap increases. This slows down device.

Lect# 1

Linear and Sat are the most confusing regions for students

$$V_{DSAT} \equiv V_{GS} - V_T \equiv V_{OD} \quad (\text{Razavi: overdrive voltage})$$

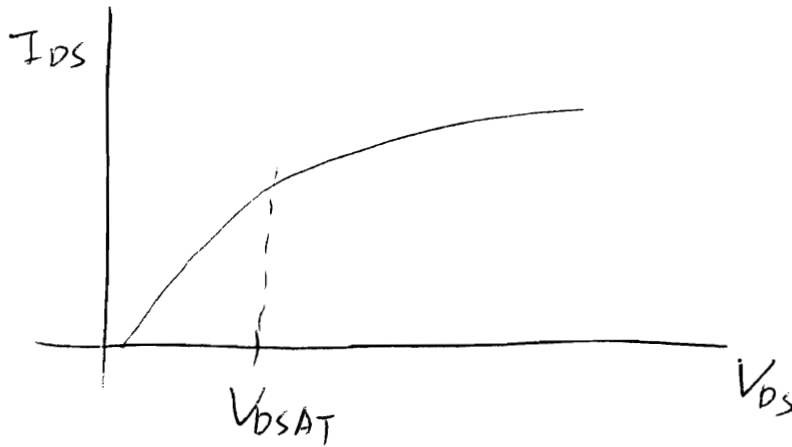
V_{OD} or V_{OV}



V_{OV} is the driving force for I_{DS} in Sat region.

Linear: $V_{DS} < V_{DSAT}$

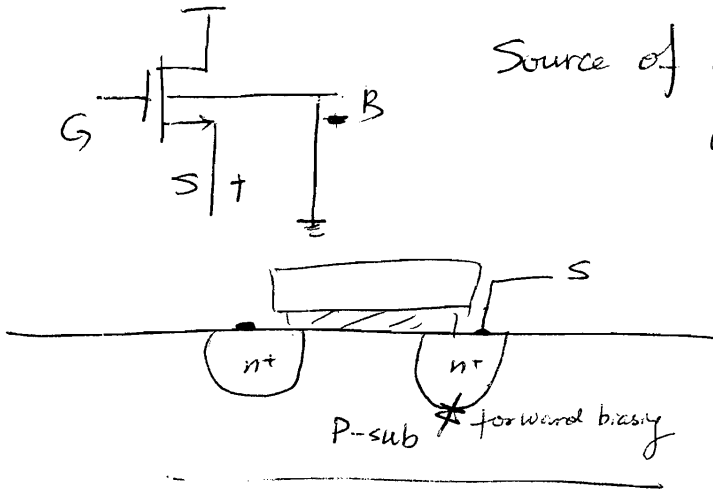
SAT: $V_{DS} > V_{DSAT}$



if V_{SB} is big enough,

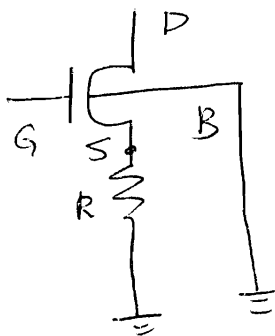
$$V_T = V_{T0} + \gamma \cdot (\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f})$$

$$\approx V_{T0} + \gamma \sqrt{V_{SB}}$$



Source of nmos should be above ~~source~~ body
 We don't use pn junction forward biasing in CMOS technology (bipolar does!)

So: $V_{SB} \geq 0$



$$I_{DS} \uparrow \rightarrow V_{SB} \uparrow \rightarrow V_T \uparrow \rightarrow I_{DS} \downarrow$$

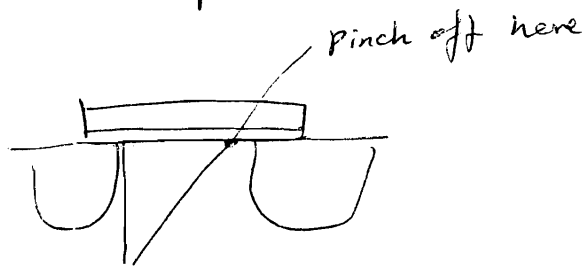
Short Channel Effect (λ)

SP-7

- ①. When $V_{DS} > V_{GS} - V_T$ (or V_{OV} or V_{DSAT})
 we start to form a depletion region X_D is the length.
 Inside depletion region, there is no electrons.

$$E = \frac{V_{DS}}{L}$$

At source side, you have a lot of electrons
 and depleted at drain side.

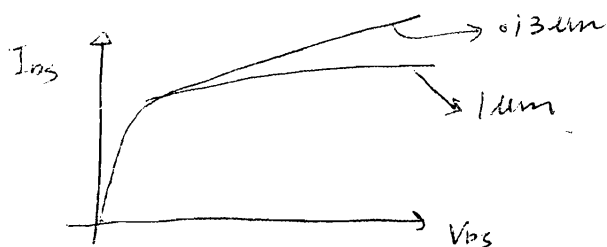
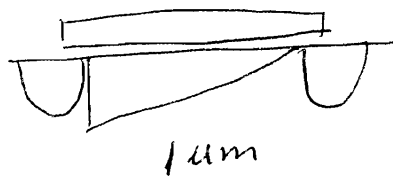
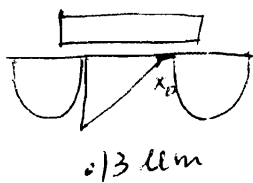


- ② when you have $L = .13 \mu m$.

$\frac{X_D}{L}$ is much larger than $L = 1 \mu m$

X_D at $.13 \mu m \approx X_D$ at $1 \mu m$.

★ And $\lambda \propto \frac{1}{L}$ at $L = 1 \mu m$



★ So even at $.13 \mu m$ technology node

we set $L = 1 \mu m$
 for analog design
 to have small λ !

★ you can not do it
 for bipolar, V_{early}
 is fixed!!!

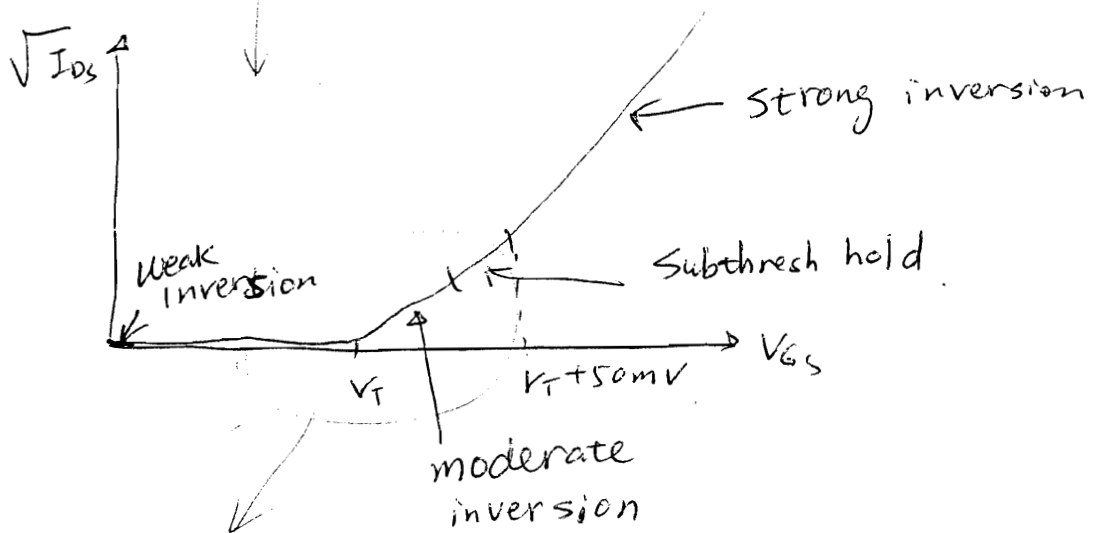
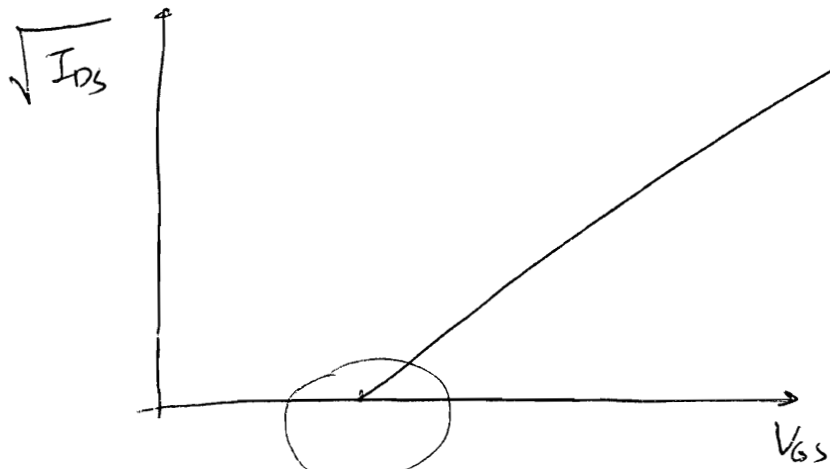
★ different from digital
 design, $L = .13 \mu m$
 keep small to save area.

$$\frac{W}{L} = 10 = \frac{1.3}{.13} \Leftarrow \text{digital.}$$

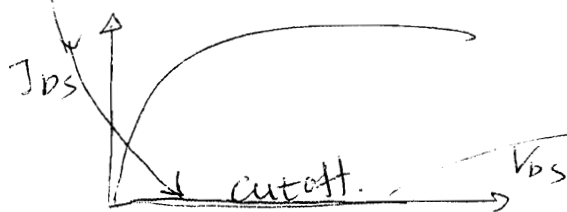
$$\frac{W}{L} = 10 = \frac{13 \mu\text{m}}{1.3 \mu\text{m}} \Leftarrow \text{analog.}$$

$$I_{DS} = I_0 e^{\frac{V_{GS} - V_T}{V_{thermal}}} \quad \text{subthreshold hold.}$$

$$V_{thermal} = kT = 26 \text{ mV} = .026 \text{ V.}$$



you always assume $I_{DS} \approx 0$ here!



can be really flat!
 not much use for this class! may be interesting to some designers

Lec # 1

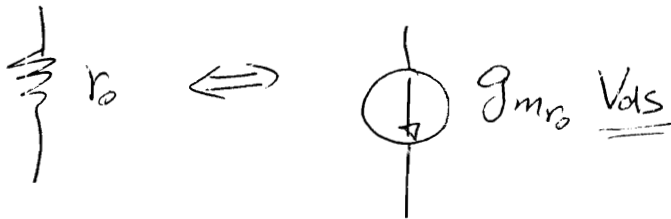
$$I_{DS} = \frac{k'}{2} \frac{W}{L_{eff}} \cdot (V_{GS} - V_T)^2$$

$$\text{or } I_{DS} = \frac{k'}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

including λ

$$\frac{dI_{DS}}{dV_{DS}} = \lambda \cdot \frac{k'}{2} \frac{W}{L} (V_{GS} - V_T)^2 \doteq \lambda \cdot I_{DS}$$

$$g_{m_{r_0}} = \frac{dI_{DS}}{dV_{DS}} = \frac{1}{r_0}$$



$V_{ds} = \Delta V_{DS}$
small letters

$$\Rightarrow r_0 = \frac{1}{\lambda I_{DS}}$$

Try to find g_m yourself! $g_m \doteq \sqrt{2k' \frac{W}{L} I_{DS}}$
 $\lambda \rightarrow 0$

V_{DSAT} vs. g_m

$$V_{DSAT} = \sqrt{\frac{2 I_{DS}}{k' W/L}}$$

$I_{DS} \uparrow \Rightarrow g_m \uparrow \Rightarrow V_{DSAT} \uparrow \Rightarrow g_m \uparrow$

LEC# 1

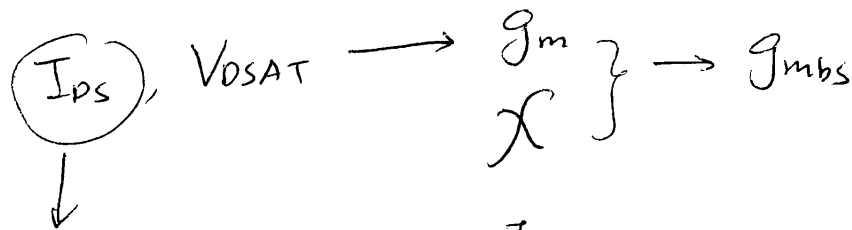
$$g_{mbs} = \chi \cdot g_m$$

$$\boxed{\frac{g_{mbs}}{g_m} = \chi}$$

$$\boxed{\chi = \frac{\gamma}{\sqrt{2 \cdot (2\phi_f + V_{SB})}}}$$

with $V_{SB} \Rightarrow$ a small value
 χ is almost fixed

The order of parameters:



Everything depends on I_{D_S}

So you need to start design by choosing I_{D_S}

saying 15 μA
 10 μA
 etc...

I_{D_S} small \rightarrow g_m small \rightarrow g_{mbs} small $\rightarrow r_o \rightarrow \infty$

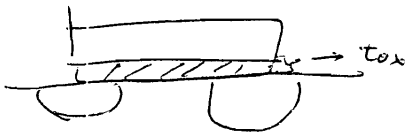
Is this good?

Too slow !!!

Bad for high freq.

$$k' = \mu C_{ox}$$

$$C_{ox} = \frac{\epsilon_{SiO_2}}{t_{ox}}$$



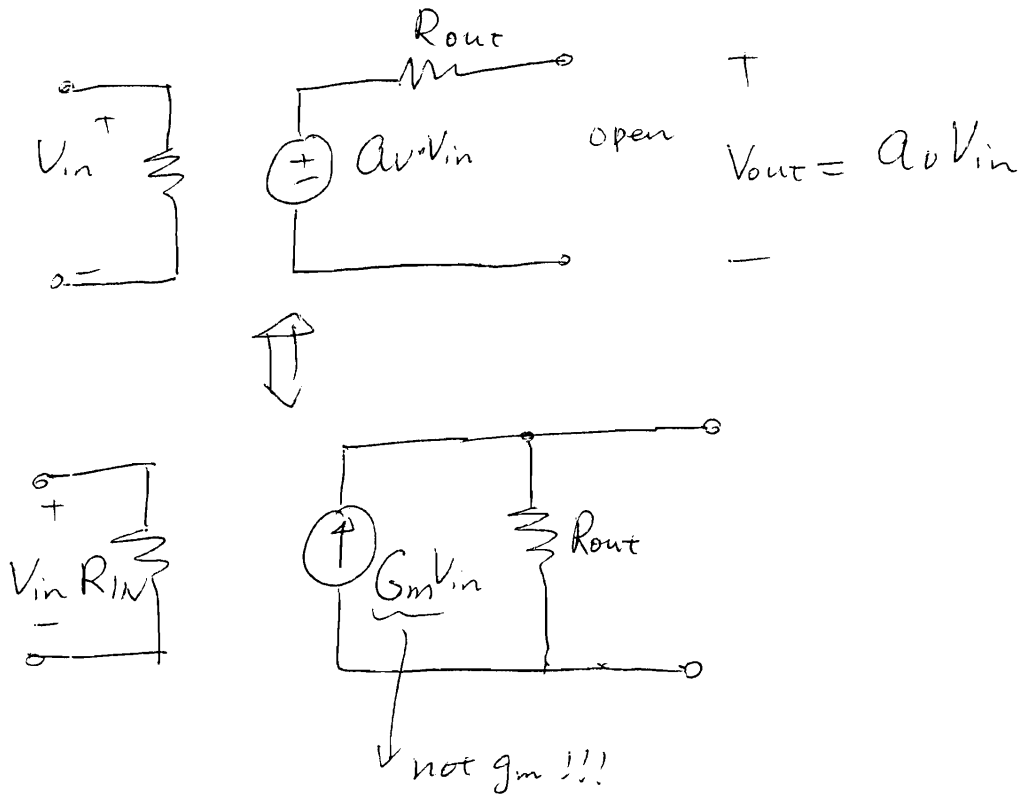
$$t_{ox} \downarrow \rightarrow C_{ox} \uparrow \rightarrow k' \uparrow \rightarrow I_{ps} \uparrow \rightarrow g_m \uparrow$$

$$\mu_p = \frac{1}{3} \mu_n$$

pmos : holes carry current

nmos : electrons carry current.

For the next several lectures:



$$V_{out} = G_m R_{out} V_{in}$$

$$V_{out} = a_v V_{in}$$
