

ECE 304 Homework 4

1. Assume $(W/L)_{1,2}=50\mu\text{m}/0.5\mu\text{m}$, $R_1=1\text{ k}\Omega$, $R_2=10\text{ k}\Omega$, $V_{DD}=3\text{ V}$, and the dc level of V_{in} and V_{out} are equal. (use the device data shown in Table 2.1, Razavi, p. 37)
 - (a) Calculate the voltage gain and the output impedance of each circuit.
 - (b) Calculate the sensitivity of each circuit's output with respect to the supply voltage. That is, calculate the small-signal "gain" from V_{DD} to V_{out} .
 - (c) Verify (a)-(b) with HSPICE using the .TF analysis option.

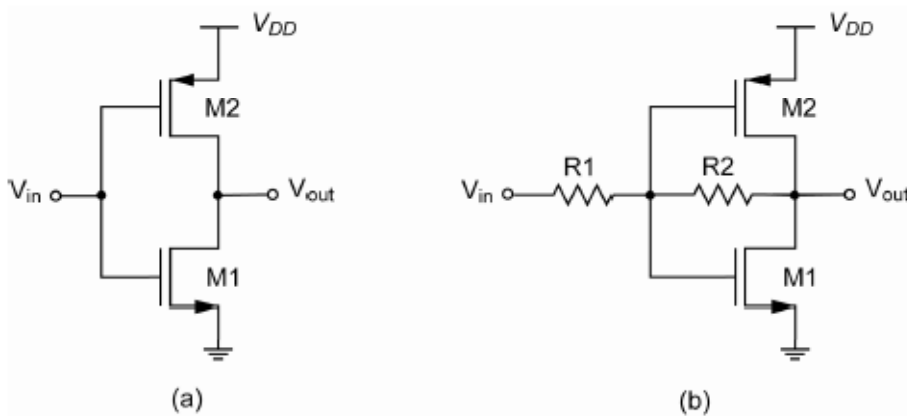


Table 2.1 Level 1 SPICE Models for NMOS and PMOS Devices.

NMOS Model

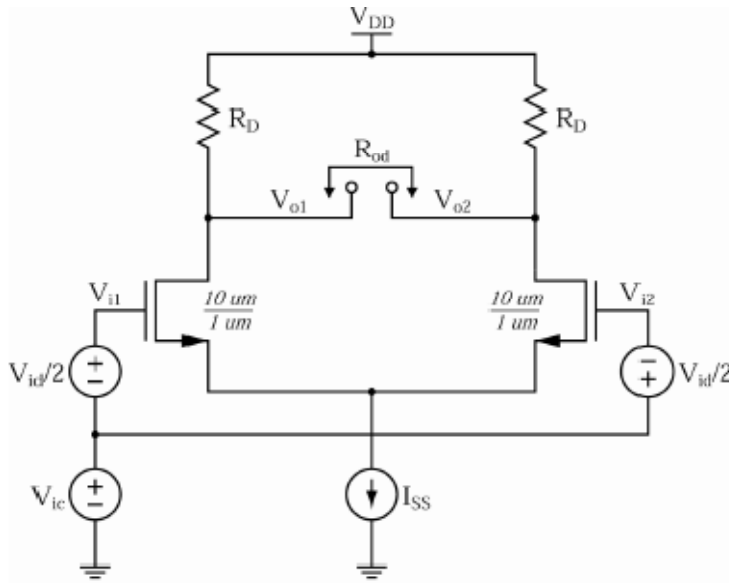
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e-6	UO = 350	LAMBDA = 0.1
TOX = 9e-9	PB = 0.9	CJ = 0.56e-3	CJSW = 0.35e-11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e-9	JS = 1.0e-8

PMOS Model

LEVEL = 1	VTO = -0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e-6	UO = 100	LAMBDA = 0.2
TOX = 9e-9	PB = 0.9	CJ = 0.94e-3	CJSW = 0.32e-11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e-9	JS = 0.5e-8

2.

In the below circuit, use $V_{DD}=1.8\text{ V}$, $I_{SS}=14\text{ }\mu\text{A}$, $R_D=100\text{ k}\Omega$, $W=10\text{ }\mu\text{m}$, $L=1\text{ }\mu\text{m}$. The device models are given at the end of the assignment.



(a) Calculate V_{DS} of the two transistors by hand, with $V_{ic}=0.9$ V, $V_{id}=0$ V, and verify with HSPICE.

(b) Plot $V_{od}=(V_{o1}-V_{o2})$ vs. V_{id} , with $V_{ic}=0.9$ V over the range $-1.8 < V_{id} < +1.8$ V.

(c) Plot $V_{oc}=(V_{o1}+V_{o2})/2$ vs. V_{ic} , with $V_{id}=0$ V over the range $0 < V_{ic} < +1.8$ V.

Use SPICE to get these plots. If there are any breakpoints in these plots, explain what causes them and calculate their positions by hand.

(d) Calculate A_{dm} with $V_{ic}=0.9$ V, $V_{id}=0$ V. Over what range of V_{id} will the gain remain high? Why does the gain drop off?

(e) Calculate A_{cm} with $V_{ic}=0.9$ V, $V_{id}=0$ V.

(f) Calculate R_{od} with $V_{ic}=0.9$ V, $V_{id}=0$ V.

Verify (d)-(f) with HSPICE using the .TF analysis option.

3. Repeat problem 2 but replace the I_{SS} current source with a resistor which results in the same I_{DS} current when $V_{ic}=0.9$ V and $V_{id}=0$ V

Use the following NMOS and PMOS transistor model for both problem 2 and 3.

```
.model nch nmos LEVEL=1 TOX=2.5n VTO=0.5 KP=140.0e-6 LAMBDA=0.1
+GAMMA=0.5 PHI=0.6
```

```
.model pch pmos LEVEL=1 TOX=2.5n VTO=-0.5 KP=65.0e-6 LAMBDA=0.15
+GAMMA=0.5 PHI=0.6
```