

2.5. Sketch I_X and the transconductance of the transistor as a function of V_X for each circuit in Fig. 2.42 as V_X varies from 0 to V_{DD} . For part (a), assume V_X varies from 0 to 1.5 V.

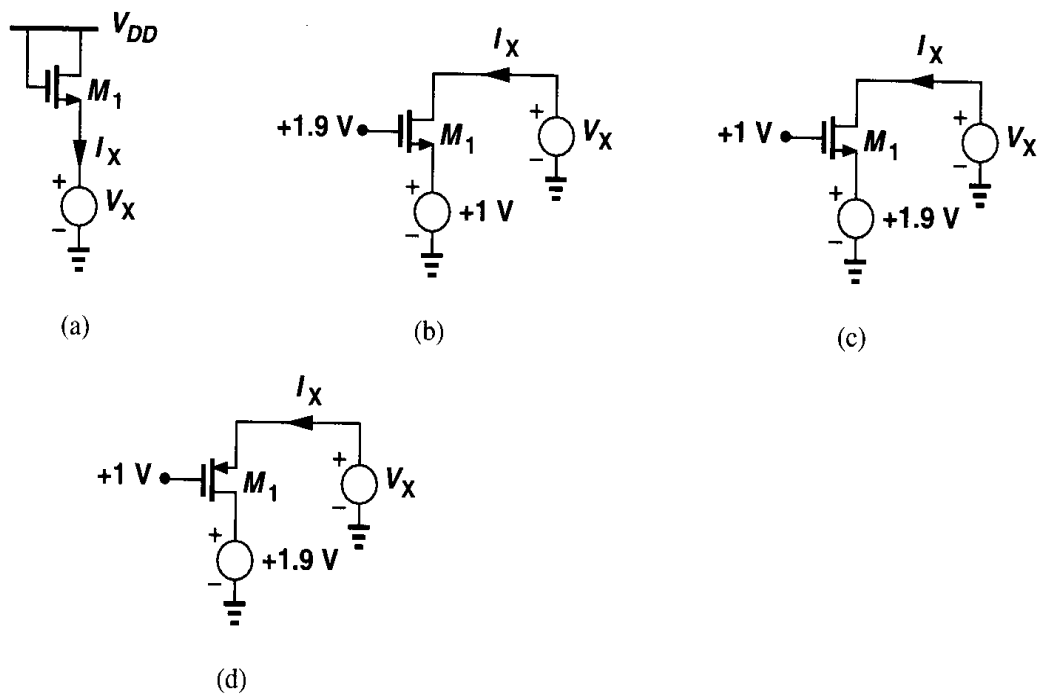


Figure 2.42

3.21. Assuming all MOSFETs are in saturation, calculate the small-signal voltage gain of each circuit in Fig. 3.73 ($\lambda \neq 0, \gamma = 0$).

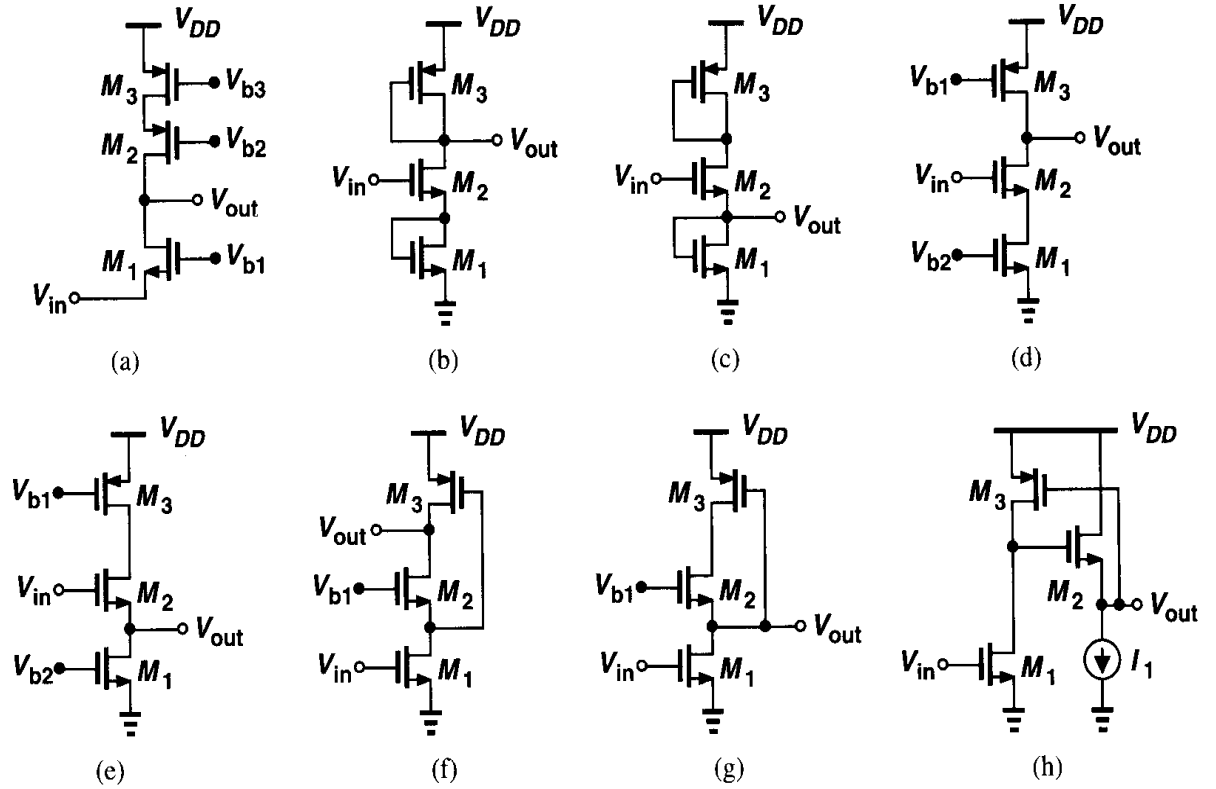


Figure 3.73

Table 2.1 Level 1 SPICE Models for NMOS and PMOS Devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e-6	UO = 350	LAMBDA = 0.1
TOX = 9e-9	PB = 0.9	CJ = 0.56e-3	CJSW = 0.35e-11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e-9	JS = 1.0e-8
PMOS Model			
LEVEL = 1	VTO = -0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e-6	UO = 100	LAMBDA = 0.2
TOX = 9e-9	PB = 0.9	CJ = 0.94e-3	CJSW = 0.32e-11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e-9	JS = 0.5e-8

VTO: threshold voltage with zero V_{SB} (unit: V)

GAMMA: body effect coefficient (unit: $V^{1/2}$)

PHI: $2\Phi_F$ (unit: V)

TOX: gate oxide thickness (unit: m)

NSUB: substrate doping (unit: cm^{-3})

LD: source/drain side diffusion (unit: m)

UO: channel mobility (unit: $\text{cm}^2/\text{V}/\text{s}$)

LAMBDA: channel-length modulation coefficient (unit: V^{-1})

CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)

CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)

PB: source/drain junction built-in potential (unit: V)

MJ: exponent in CJ equation (unitless)

MJSW: exponent in CJSW equation (unitless)

CGDO: gate-drain overlap capacitance per unit width (unit: F/m)

CGSO: gate-source overlap capacitance per unit width (unit: F/m)

JS: source/drain leakage current per unit area (unit: A/m^2)