

Introduction

Technology In Our Everyday Lives

- Semiconductor Industry forecasts \$252 billion in sales for 2007



Computers



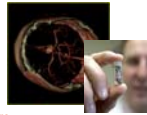
Military



Automotive
20-80 microprocessor controlling break systems, airbags, infotainment, safety, driver assistance, etc.



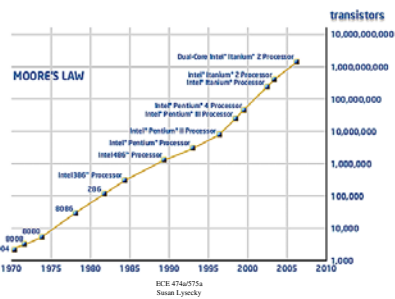
Entertainment



Healthcare
Smart Pills electronically track and instructed to deliver medicine to specific location, better imaging, remote surgery, etc.

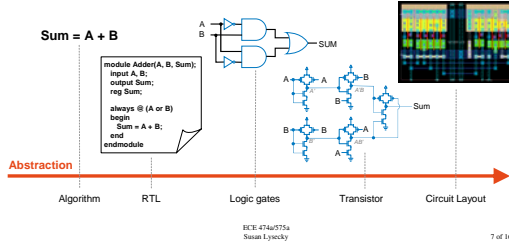
Moore's Law

- Doubling of IC capacity every 18 months
 - Gordon Moore predicted trend in 1965 and continues today



Increasing Abstraction

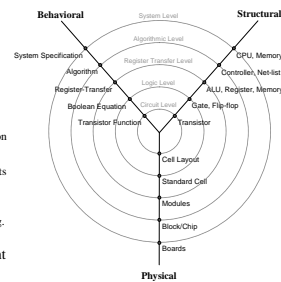
- Higher abstraction level simplify designer effort
 - Description smaller/easier to capture
 - Don't have to know/remember the low-level details
 - Many more possible implementations available



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Y-chart

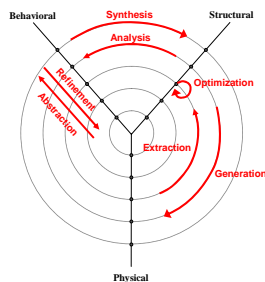
- Representation proposed by Gajski in 1983 (other variations exist)
 - Captures the relation between different design activities
- Each axis represents type of description
 - Behavioral**
 - Defines function of a circuit regardless of its implementation
 - Structural**
 - Interconnections of components with known behavior
 - Physical**
 - Relates to physical objects (e.g. transistors) of the design
- Within domain there are different abstractions



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Y-chart Transformations

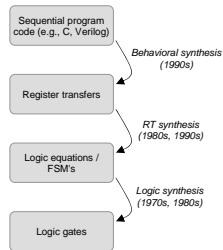
- Refinement**
 - Transformation of high-level description to a lower-level description (more detail)
- Abstraction**
 - Associating a higher-level behavior to hide complex inner details
- Synthesis**
 - Process that transforms description of circuit behavior into a structural implementation
- Analysis**
 - Abstracting how circuit performs task to what is the overall goal
- Optimization**
 - Transformation that improves criteria of interest to us (area, delay, cost)
- Generation**
- Extraction**



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Why CAD?

- Computer-Aided Design (CAD)
 - Large scale management through abstraction
 - Design optimization
 - Reduced design time
 - Bridges the gap between different views of abstractions/domains
- Hardware design evolution
 - Logic synthesis
 - Converts logic equations or FSMs into gates
 - Register-transfer (RT) synthesis
 - Converts FSMs into FSMs, logic equations, structural components (registers, adders, ALUs)
 - Behavioral synthesis
 - Converts sequential programs into FSMs



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Course Overview

- Design Specification
 - Structural vs. Behavioral
 - Design and implementation of sequential circuits – RTL (Register-Transfer Level) Design
 - C to gates
- Optimization Techniques
 - Optimization and tradeoffs of combinational and sequential circuits
 - Heuristic minimization of two-level circuits
 - Representation of logic functions - Binary decision diagrams (BDDs), ESSPRESSO file format
- CAD Tools
 - Utilize industry standard tools to simulate (synthesizable) designs
 - Develop optimization tools

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Course Syllabus – General Info

- Instructor Information
 - Susan Lysecky, slysecky@ece.arizona.edu
 - Office Hours: W 9:30-10:30, F 1:00-2:00, or by appointment.
 - Office: ECE 356C
- Lecture
 - MWF 12:00PM-12:50PM, CHEVEZ 111
 - Course Website: <http://www.ece.arizona.edu/~ece474a>
- Textbook
 - No required textbook (see me if you want the reference materials)

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Course Syllabus - Grading

- Grading will be evaluated on an individual basis. You will not be competing with other students for your grade. If all students do well in the class, everyone will get an A. Your grade is dependent on the effort you put into the class. Letter grades will be assigned as follows: 90% and above is an A, 80% and above is a B, 70% and above is a C, 60% and above is a D, and less than 60% is an E.
- The grading is based on a weighted sum as follows:
 - 65% Exams (4 Exams, lowest score dropped)
 - 30% Programming Assignments (2-3 projects, not equally weighted)
 - 5% Participation/In-class exercises (ICE)
- Students enrolled in ECE 574A will have additional/different homework, exam, and programming assignment requirements.

Course Syllabus - Policies

- Punctuality: Please arrive on-time to class. If you are late, try not to disrupt others and enter as quietly as possible.
- Absence: If you miss a project deadline or exam, you need to bring written documentation (i.e. tow truck bill, receipt from doctor's office, court summons, etc.) to verify your whereabouts. You can remove any private information.
- Cell Phones: Please turn off you cell phone before you come to class.
- Academic Dishonesty: Any academic dishonesty will not be tolerated. Unless otherwise specifically stated by your instructor or teaching assistant, all course work should be done on your own. Please consult the UA Code of Academic Integrity.
 - Engineering is a social discipline requiring good people skills.
 - Study groups are strongly encouraged
 - Study for exams or practice problems, NOT for programming projects
 - If you are in doubt, don't do it!
 - I will check for similar projects
 - Academic Integrity Video - <http://deanofstudents.arizona.edu/>

Course Syllabus - Policies

- Reading: Be prepared. Read over material before class. I will however do my best to post upcoming lecture topics and the source. Check the class webpage regularly for announcements.
- Regrades: All requests for regrades must be submitted in writing within one week of the distribution of the graded material. Assignments requested to be regraded will be regraded in their entirety, which could possibly result in a lower score for the requested problem/assignment.
- Late Programming Assignments: No late assignments will be accepted unless you have already made arrangements with the instructor *before the due date*.

To do list

- Xilinx software available for download
- Extended lab hours forms – PRINT NEATLY
- Participation point 1 (1 pt) – Use electronic turnin, each person should submit group information by MON Aug 31
 - Groups are optional
 - Maximum group size is 2! You should both be in either 474a or 574a as the projects differ slightly between classes.
- Participation point 2 (1 pt) - Survey
- Participation point 3/4 (2 pts) – Fill out and return ECE 474A/574A passport posted online, return by MON Aug 31

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