

Diode model

Objective: *Introduce concepts in device modeling for circuit analysis*

Outline:

1. P-N junction diode DC model
2. Dynamic model
3. Diode equivalent circuit

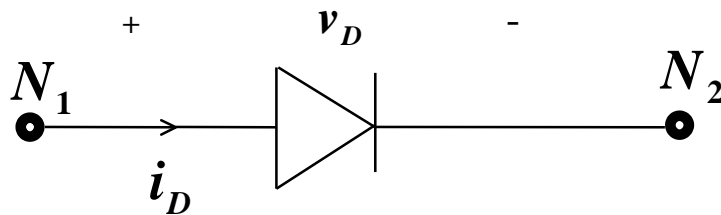
Supplemental reading:

Antognetti and Massobrio, Chapter 1

1. P-N junction diode DC model

Supporting reading: Antognetti, Massobrio, model based on P-N junction theory.

Circuit symbol



The relations are composed of: A) static model- (I-V characteristics)
A) dynamic model- (C-V characteristics).

Static model

An important constant - thermal voltage:

$$V_T = \frac{kT}{q}$$

k - Boltzmann constant, T - absolute temperature, q - electron charge.

I-V characteristic

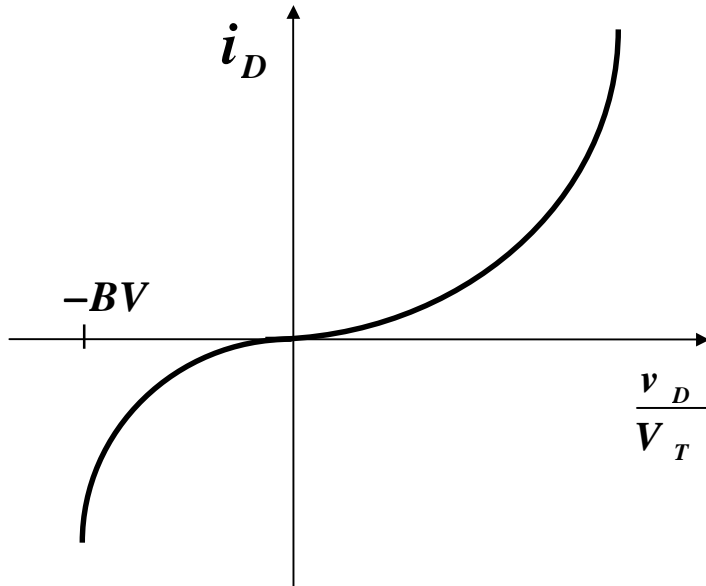
$$i_D = \begin{cases} I_s \left(e^{\frac{v_D}{nV_T}} - 1 \right) + v_D G_{\min} & ; \quad -5V_T \leq v_D \\ -I_s + v_D G_{\min} & ; \quad -BV < v_D < -5V_T \\ -I_{BV} & ; \quad v_D = -BV \\ I_s \left(e^{\frac{BV+v_D}{nV_T}} - 1 + \frac{BV}{V_T} \right) & ; \quad v_D \leq BV \end{cases}$$

Model parameters:

n - emission coefficient (empirical, $1 \leq n \leq 2$), I_s - saturation current,
 BV - break down voltage, I_{BV} - break down current,
 G_{\min} - minimum conductance (introduced to facilitate numerical calculations).

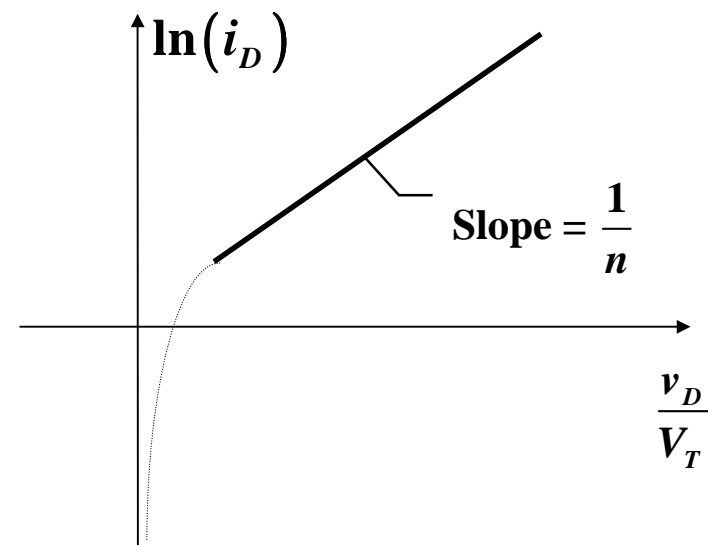
Sketches of I-V relations

Linear scale



Logarithmic scale ($v_D \geq -5V_T$)

$$\ln(i_D) = \ln(I_s) + \frac{1}{n} \frac{v_D}{V_T}$$



2. Dynamic model (describing charge storage capability)

Two components are distinguished in the charge, Q_D , stored in a diode

$$Q_D = Q_s + Q_d$$

Q_s - the charge stored in the neutral regions (NR), formed by minority carriers injected into NR. This charge is determined by the formula

$$Q_s = \tau_D i_D$$

where τ_D is the transit time, a model parameter.

Q_d - the depletion region charge, also called the junction charge or space charge.

The model of junction charge is based on approximate theory of abrupt P-N junction. The model of junction charge can be represented in the integral form

$$Q_d = C_{do} \int_0^{v_D} \left(1 - \frac{v}{\Phi_o} \right)^{-m} dv$$

where: m - is the grading coefficient (empirical, $\frac{1}{3} \leq m \leq \frac{1}{2}$),

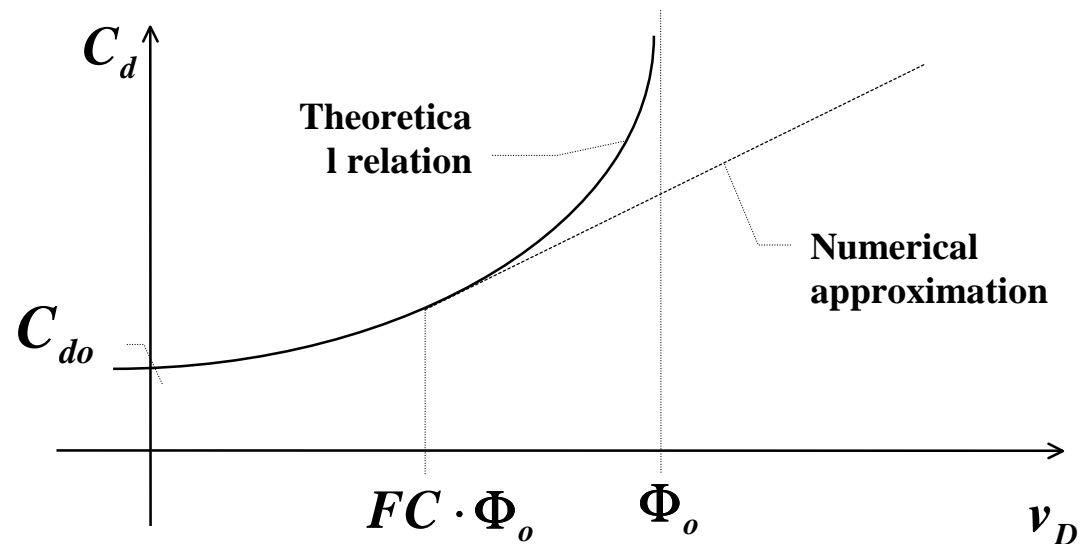
Φ_o - is the junction built-in potential, C_{do} - is the zero bias junction capacitance.

Note: C_{do} - as a zero bias junction capacitance is often denoted by C_{jo} . This is an incremental capacitance

The diode charge storing capability in the depletion region can alternatively be represented by an incremental capacitance

$$C_d = \frac{dQ_d}{dv_D} = C_{do} \left(1 - \frac{v_D}{\Phi_o} \right)^{-m} .$$

The model of depletion charge is discontinuous at $v_D = \Phi_o$. In practice $v_D < \Phi_o$ and theoretically there is no problem with this discontinuity. However, in actual computations, due to numerical errors it is possible that $v_D \geq \Phi_o$ and the model has to be modified. A modification used in SPICE is explained in the figure below:



The parameter FC determines the diode potential assumed as a fraction ($0 < FC < 1$) of built in voltage, Φ_o , above which the diode C-V characteristic is represented a linear function of the bias voltage.

The linear approximation is constructed in such a way that at $v_D = FC \cdot \Phi_o$ begins at the capacitance determined by the theoretical curve and its slope is determined by the slope of the tangent to the theoretical curve at the break point $v_D = FC \cdot \Phi_o$.

The modified model of the junction charge is

$$Q_d = \begin{cases} C_{do} \int_0^{v_D} \left(1 - \frac{v}{\Phi_o}\right)^{-m} dv & ; \quad v_D < FC \cdot \Phi_o = \Phi^* \\ C_{do} \left[F_1 + \frac{1}{F_2} \int_{\Phi^*}^{v_D} \left(F_3 + \frac{mv}{\Phi_o} \right) dv \right] & ; \quad v_D \geq \Phi^* \end{cases}$$

The constants, F_1 , F_2 , F_3 , determined mathematically by the above specified condition of approximation are:

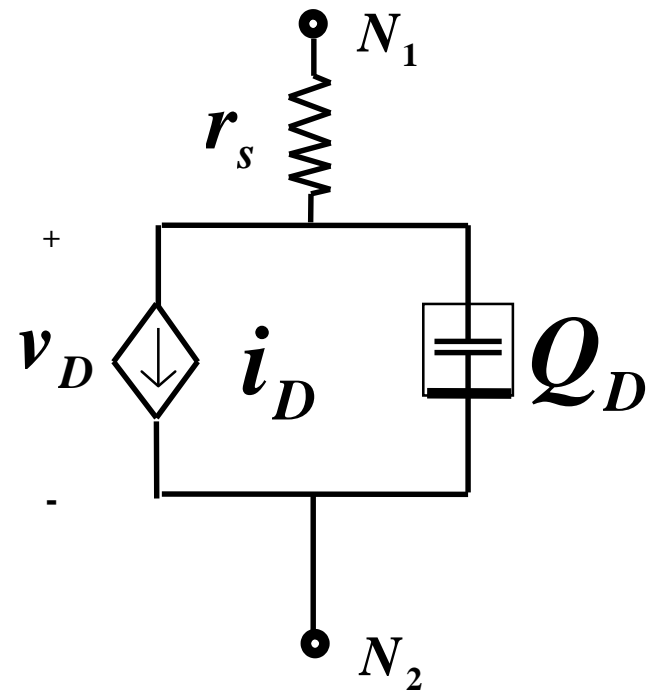
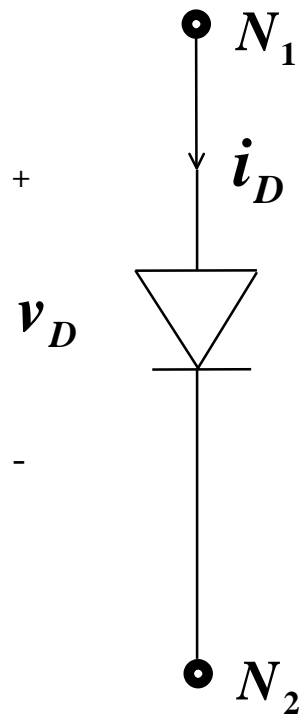
$$F_1 = \frac{\Phi_o}{1-m} \left[1 - (1-FC)^{1-m} \right]$$

$$F_2 = (1-FC)^{1+m} \quad \cdot$$

$$F_3 = 1 - FC(1+m)$$

3. Diode equivalent circuit

It is convenient to represent the model in the form of equivalent circuit shown below (models of transistors are also represented using suitable equivalent circuits)



Summary of model parameters (SPICE)

5 static model parameters:

I_s - saturation current, BV - break down voltage, IBV - break down current, n - emission coefficient, r_s - resistance of neutral regions.

Numerical constant

G_{\min} - minimum conductance (constant selected for numerical reasons, *same for all elements*).

5 dynamic model parameters:

τ_D - transit time, C_{do} - zero-bias junction capacitance, Φ_o - built-in voltage, m - grading coefficient, FC - fraction of built-in voltage used as a delimiter between nonlinear and linear sections of C-V characteristic.