

PMD Compensation using LDPC Coding based Turbo Equalization

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Abstract: An iterative equalization scheme suitable for electronic PMD compensation based on BCJR equalizer and a novel class of LDPC codes is proposed. The first order PMD with differential group delay up to two bit-periods can be completely compensated for.

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In this paper, a particular turbo equalization [1] scheme suitable for electronic polarization mode dispersion (PMD) compensation based on Bahl, Cocke, Jelinek and Raviv (BCJR) [2] equalizer, and a novel class of low-density parity-check (LDPC) codes is proposed. A significant benefit of using the BCJR equalizer [3], compared to Viterbi equalizer, is that in addition to detected bits it also provides bit reliabilities, i.e. soft decisions. Iterative decoding and LDPC coding is currently the most advanced forward error correction (FEC) approach, but its power can be fully exploited only if the soft bit reliabilities are supplied to the decoder. We show that for reasonable BCJR equalizer complexity, the first order PMD with differential group delay up to two bit-periods can be completely compensated for. Notice that turbo equalization based on *convolutional codes* has already been considered for PMD compensation [4], however, those schemes exhibit error floor phenomena as shown in [4]. In several recent papers (see [5], and references therein), we have shown that iteratively decodable LDPC codes outperform turbo product codes in bit-error rate performance. The decoder complexity of these codes is comparable to (or lower than) that of turbo product codes, and significantly lower than that of serial/parallel concatenated turbo codes. For reasons mentioned above, LDPC code is a viable and attractive choice to be used for turbo equalization of polarization-mode dispersion. The extrinsic information transfer (EXIT) chart analysis [6] is used to select the LDPC codes suitable for turbo equalization of PMD. To facilitate the implementation at high-speed a novel class of LDPC codes designed using the product of orthogonal arrays [7] is introduced.

The return-to-zero on-off keying (RZ OOK) receiver configuration is given in Fig. 1. The turbo equalizer (see Fig. 1) is composed of two components: (a) the BCJR equalizer, and (b) LDPC decoder. The main idea is to use the BCJR equalizer to partially cancel the ISI due to PMD to reduce the BER down to 10^{-3} - 10^{-4} , and feed the log-likelihood ratios (LLRs, channel bit reliabilities) obtained from BCJR equalizer into iterative decoder of an LDPC code. If a valid codeword is reached decoding halts, otherwise, the sum-product LDPC decoder starts decoding by taking the produced BCJR LLRs as inputs. We refer to this step as an *outer iteration*, to differentiate it from iterations within the sum-product algorithm, which are referred to as *inner iterations*. The LDPC decoder iterates until a valid codeword is obtained or a pre-defined number of iterations has been reached. The *extrinsic* LLRs of the LDPC decoder (the difference of LDPC decoder output and input LLRs) are passed back to the BCJR equalizer as inputs. The BCJR equalizer processes the samples and LDPC decoder extrinsic LLRs, to provide the initial bit reliabilities (LLRs) for the LDPC decoder. Therefore, the *extrinsic soft information* is iterated between BCJR equalizer and LDPC decoder a certain number of times in a fashion similar to the *turbo decoding*. Notice that in proposed turbo equalizer *we do not use the interleaver* (commonly used in turbo equalization schemes, e.g., [1],[4]), to reduce the processing delay and facilitate the implementation at high-speed. The BCJR equalizer operates on a *trellis* that is a *discrete dynamical model* of the optical channel (see our recent article [3]). For the first order PMD, the optical channel responses $h_H(t)$ and $h_V(t)$ corresponding to the horizontal and vertical principal states of polarizations (PSPs) are given respectively as [4] $h_H(t)=\delta(t+\Delta\tau/2)$ and $h_V(t)=\delta(t-\Delta\tau/2)$, where $\Delta\tau$ is the differential group delay (DGD) of two PSPs.

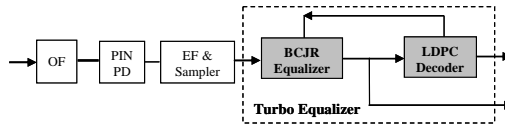


Fig. 1 Receiver and PMD compensator architectures (OF-optical filter, PD-photodetector, EF-electrical filter)

We are turning our attention now to the design of LDPC code suitable for use in turbo equalization of PMD. The LDPC codes employed in this paper are designed based on the *product of 1 orthogonal arrays*, the concept introduced by K. A. Bush in 1952 [7]. We have shown in [8] that the combinatorial objects known as orthogonal

arrays (OAs) (see [7] or [8] for definition) can be used to design the LDPC codes. To keep the code rate above 0.8 we had to delete some of the classes from an orthogonal array. The high-rate (>0.9) LDPC codes based on product of OAs can easily be designed without a need for deletion of some of the classes in an orthogonal array. The code rate (R) of an LDPC code designed using the concept of product of orthogonal arrays is lower bounded by

$$R = \frac{N - \text{rank}(H)}{N} \leq 1 - \frac{\min(k_1, k_2, \dots, k_l) q_1 q_2 \dots q_l}{N_1 N_2 \dots N_l}, \quad (1)$$

where with N_i , k_i , and q_i we denoted the size, constraint and number of levels of i th ($i=1, \dots, l$) OA, and with $N=N_1 \dots N_l$ the size of product of OAs. (With $\text{rank}(H)$ we denoted the rank of a parity-check matrix H). Since the product of sizes grows much faster than product of levels (in Eq. (1)) the high code rates LDPC codes can easily be designed. For example, the LDPC code designed using the product of OA(49,8,7,2) and OA(169,14,13,2) has the rate 0.9129, and the codeword length 8281. The girth (the shortest cycle in corresponding bipartite graph [5]) of the proposed LDPC codes is at least six.

The results of simulations are shown in Fig. 2 for two different DGD values: (a) $\Delta\tau/T=1.0$ (T -the bit period), and (b) $\Delta\tau/T=2.0$; and different memories in the trellis. RZ-OOK of a duty cycle of 33% is observed, the launched power is set to 0dBm, and the extinction ratio to 14dB. The bandwidth of optical filter is set to $3/T$, and the bandwidth of electrical filter to $0.65/T$. Three classes of LDPC codes are considered in simulations. The first class is the girth-8 regular LDPC code (8547,6922) of rate 0.81. The second class are regular girth-6 LDPC codes designed based on product of two orthogonal arrays: (a) LDPC(8281,7560) of code rate 0.913 (based on product of OA(49,8,7,2) and OA(169,14,13,2)), and (b) LDPC(4096,3813) code of rate 0.93 (based on product of OA(16,5,4,2) and OA(256,17,16,2)). The third class is girth-6 *irregular* LDPC(3315,3032) code of rate 0.915 obtained from product of OA(16,5,4,2) and OA(256,17,16,2) by judiciously removing the entries in the product OA. For DGD $\Delta\tau/T=1.0$ the BCJR equalizer for trellis memories $2m+1=3$ and $2m+1=5$ gives the comparable BER performance, while for $2m+1=7$ starts to perform better below 10^{-3} . Notice the optimum threshold receiver enters the error floor, and any advanced FEC *alone* is not able to operate for that DGD. For trellis memory $2m+1=7$ the coding gain improvement of LDPC codes from second class (of code rate above 0.9) over the BCJR equalizer is about 7.5 dB, while the girth-8 code of rate 0.81 provides the coding gain about 10dB; both at BER of 10^{-6} . For DGD $\Delta\tau/T=2.0$ even the BCJR equalizer for trellis memory $2m+1=3$ enters the error floor, while for larger trellis memories it is able to operate properly. The coding gain improvement of girth-8 code of rate 0.81 over the BCJR equalizer with trellis memory $2m+1=7$ is around 10.8 dB at BER of 10^{-6} . At BER of 10^{-12} much larger coding gains are expected. The simulations are performed for 5 outer iterations and 25 sum-product algorithm inner iterations. Notice that turbo equalization schemes based on convolutional codes and interleavers exhibit the severe error flooring around 10^{-6} (e.g. Fig. 17 in [4]), and require additional outer RS code to deal with the error floor phenomena. Notice also that proposed LDPC codes based turbo equalization scheme is able to operate even at DGDs above $\Delta\tau/T=2.0$ for reasonable complexity in BCJR equalizer trellis.

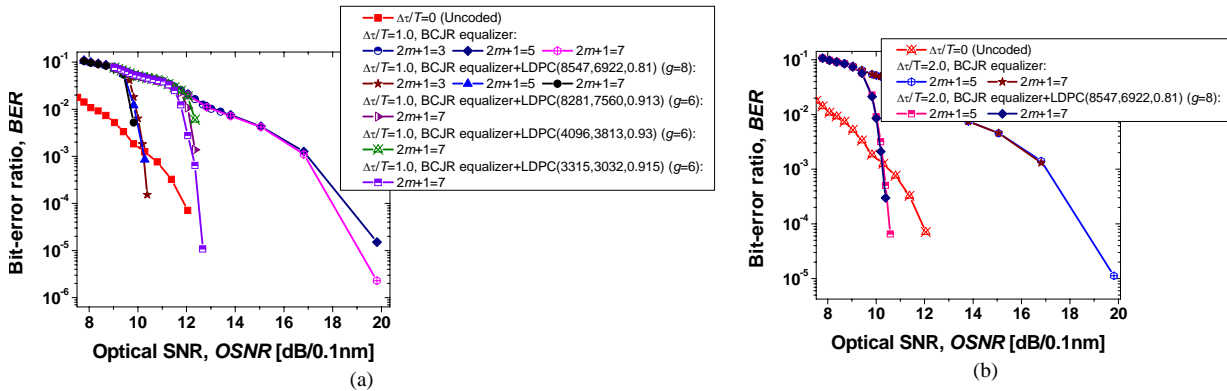


Fig. 2 BER performance of PMD turbo equalizer for different LDPC codes, and two different values of DGD: (a) $\Delta\tau/T=1.0$, and (b) $\Delta\tau/T=2.0$.

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