Lowering the Error-Rate Floors of Moderate-Length High-Rate Irregular LDPC Codes[1]

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Abstract — **This paper presents a specialized class of irregular low-density parity-check (LDPC) codes of moderate length ($10^3 \leq n \leq 10^4$) and high rate ($R \geq 3/4$). Codes in this class admit low-complexity encoding and have lower error rate floors than other irregular LDPC code design approaches. It is also shown that this class of LDPC codes is equivalent to a class of systematic serial turbo codes. Code designs of moderate-length, high rate codes which yield bit error rate floors below 10^{-8} are presented.**

I. Introduction

Most of the recent literature on LDPC codes has focused on long, low-rate codes. Our goal is the design of codes superior in performance to alternative approaches and which allow low-complexity encoding and decoding and very low error-rate floors. We make some novel modifications to the work of Richardson *et al.* [1] which constrains our codes to a specialized class of irregular LDPC codes. These modifications improve performance for the regime of n and R space under consideration and lead to vastly simplified encoders.

II. The Specialized Class of LDPC Codes

Lemma. In a given Tanner graph (equivalently, H matrix), the maximum number of degree-two v-nodes possible before a loop is created involving only these nodes is $N_{v,\max}(2) = n - k - 1 = m - 1$. Furthermore, for codes possessing this maximum, the submatrix of H composed of only its weight-two columns is simply a permutation of the following $m \times (m-1)$ parent matrix

$$T = \begin{pmatrix} 1 & & & \\ 1 & 1 & & \\ & \ldots & \ldots & \\ & & 1 & 1 \\ & & & 1 \end{pmatrix} \quad (1)$$

We are interested in the maximum number of loop-free weight-two columns because the optimal v-node degree distribution (for code rate greater than 1/2) usually implies $N_{v,opt}(2) > m - 1$. Thus, we focus on codes for which $N_v(2)$ is not at its optimum, but is instead at the smaller value prescribed by the Lemma.

Consider now the parity-check matrix H given by

$$H = (H_1 \; H_2) \quad (2)$$

where H_1 is a sparse $(n-k) \times k$ matrix containing no weight-two columns and H_2 is a full-rank $m \times m$ matrix created from T by appending to it (on the right) a weight-one column vector with a '1' at the bottom.

Thus, the code may be interpreted as a systematic block-oriented serial turbo code whose encoder is depicted in Fig. 1. Further, encoding may be simply accomplished in a recursive fashion using the H matrix. These code may be called extended irregular repeat-accumulate (IRA) codes as they correspond to slight generalizations of IRA codes [2] [3] .

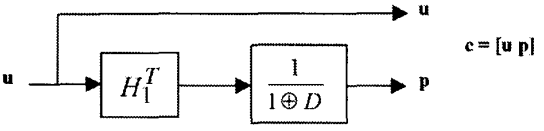

Figure 1: Turbo-like efficient encoder.

III. Code Design Results

Example In this example, we compare the performance of four $n = 4161$ rate-0.82 LDPC codes:

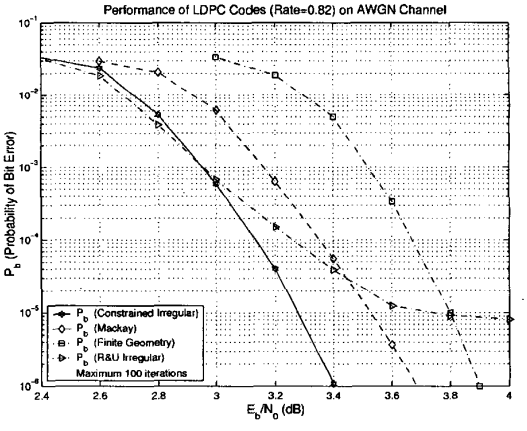

Figure 2: Performance comparison of LDPC codes.

References

[1] T. Richardson, A. Shokrollahi, and R. Urbanke, "Design of capacity-approaching irregular low-density parity-check codes," *IEEE Trans. Information Theory*, pp. 619-637, Feb. 2001.

[2] H. Jin, A. Khandekar, and R. McEliece, "Irregular repeat-accumulate codes," *2nd International Symposium on Turbo Codes & Related Topics*, pp. 1-8, Brest, France, Sep. 2000.

[3] R. Narayanaswami, "Coded Modulation with Low-Density Parity-Check Codes," M.S. thesis, Texas A&AM University, 2001, Chapter 7.

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