Turbo, LDPC, and RLL Codes in Magnetic Recording

William E. Ryan[a], Steven W. McLaughlin[b], Kofi Anim-Appiah[b], and Michael Yang[a]
a. University of Arizona, {ryan,yangsiz}@ece.arizona.edu
b. Georgia Institute of Technology, {swm,kofi}@ece.gatech.edu

Abstract- We survey recent research in the area of concatenated codes and iterative decoding for magnetic storage channels. We cover results on parallel and serial concatenations, low density parity check codes, and runlength limited codes.

Keywords: turbo codes, low density parity check codes, constrained codes, partial response, magnetic data storage.

1. INTRODUCTION

The magnetic recording channel (MRC) presents unique and interesting challenges to signal processing and coding engineers. The channel input is constrained to be binary and runlength-limited, and the read-back signal is subject to intersymbol interference (ISI), generally equalized to some target partial response shape. Further, as a consequence of the particular type of ISI seen, high code rates are required since the code rate loss goes as R^2 rather than R (R is the code rate). Complicating matters further is that the noise is colored, the coloration a consequence of both media noise and equalization, and errors may come in large bursts, a consequence of thermal asperities.

At present there is a great deal of activity in the magnetic recording community to determine the viability of concatenated coding and iterative decoding for future storage products. This paper surveys a number of coding approaches for magnetic storage which have been reported recently in the literature, including parallel and serial concatenations of convolutional codes (CCs), low density parity check (LDPC) codes, and runlength limited (RLL) codes.

2. CONCATENATED ERROR CONTROL CODES

Fig. 1 depicts the concatenated encoding and iterative decoding system model. The outer code can be a parallel concatenation of (recursive) convolutional codes (PCCCs), a single convolutional code, or a LDPC code. (As we will see, an interleaver is unnecessary for the LDPC case.) Other codes are possible, but we do not consider them here. Note that in each case, the partial response channel is treated as an inner code serially concatenated with the outer code. When the outer code is simply a CC, we refer to it as a serial concatenated convolutional code (SCCC) scheme.

2.1 Parallel Concatenated Schemes

The early work on turbo codes for magnetic recording consider the PCCC configuration together with the PR4 channel (modeled by the polynomial $1-D^2$) [1]. Because high code rates are a necessity for MRCs [2], high code rates (achieved by puncturing) were considered. Further, the PCCC-encoded bits were precoded with the $\frac{1}{1\oplus D^2}$ precoder so that a **1** is mapped to ± 2 and a **0** is mapped to 0 over the precoded PR4 channel. This has the effect of converting codewords with large minimum Hamming distance to channel sequences with large minimum Euclidean distance [3]. To decode, a PR4 *a posteriori probability* (APP) detector employs the BCJR algorithm to compute the log-likelihood ratio $L(c_k)$ for each code bit c_k. The PCCC decoder treats these inputs $L(c_k)$ as extrinsic information, but otherwise iterates in the usual fashion. The PR4 APP detector may or may not be included in the iterative loop.

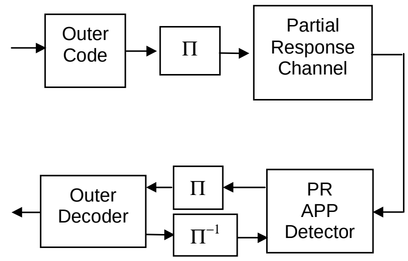

Fig.1. Coded partial response system with iterative decoding.

Fig. 2 presents simulation results for the PR4 channel with AWGN when the PR4 APP detector is not in the iterative loop. The curves are presented for 16-state PCCCs with an information-word size of 4096 bits and with 3 and 15 decoder iterations. Note the gains over the uncoded case at $P_b = 10^{-6}$ are quite substantial and far greater than any trellis code: 5-plus dB for the rate 4/5 code and 2-plus dB for the rate 64/65 code. Observe also that the well-known error-rate floor for PCC's occurs below 10^{-7} for all of the codes, although the floor appears nearby for the rate 16/17 code. The figure includes an estimate of the level of the floor for this code. When the PR4 APP detector is included in the iterative loop with the two PCC APP decoders, the gains for all rates is increased by about 0.5 dB [4].

2.2 Serial Concatenated Schemes

Shortly after the published work on parallel concatenated approaches, SCCCs were studied by a number of authors (e.g., [5], [6], [2]). These schemes

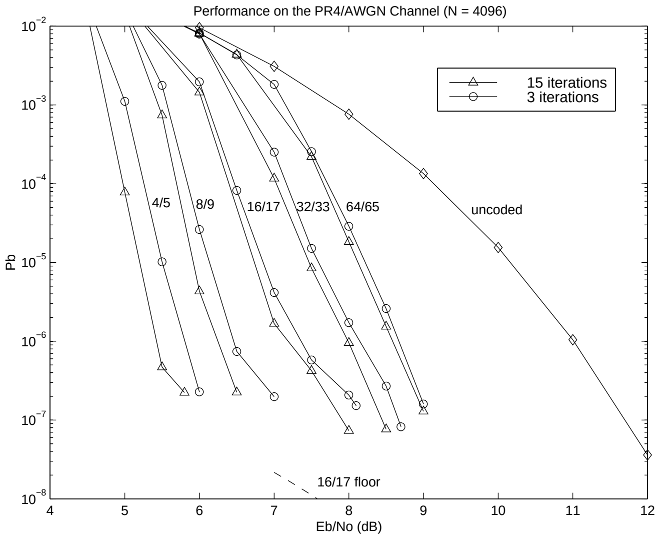

Fig. 2. Performance of the PCCC scheme (PR4).

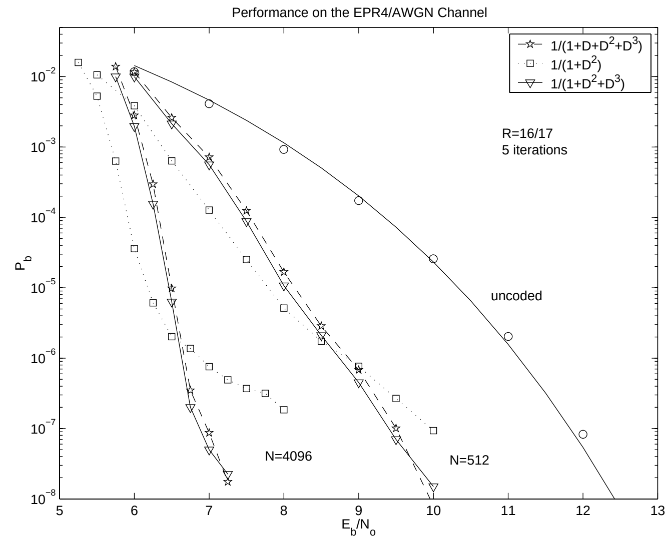

Fig. 3. Performance of the SCCC scheme (EPR4).

have the advantage that a convolutional encoder and, more importantly, an APP decoder were removed. Further, it appeared that the SCCC configuration performed slightly better than the PCCC configuration. However, a closer inspection revealed that the error rate floor for the SCCC case was significantly higher than that of the PCCC case [7]. (This should be intuitively clear since we have replaced an outer turbo code with a much weaker convolutional code.) This discovery led to some work on the design of optimal precoders and interleavers for the SCCC scheme, where optimality is in the sense of lowest error rate floor [7], [8], [9].

The approach taken to lower the error rate floor was to study the worst-case (lowest-weight) error patterns as seen by the precoded PR channel. Since the outer codes consisted of highly punctured recursive convolutional codes (RSCs), these worst-case patterns are weight-two patterns. This led to a precoder design approach involving a distance enumerator conditioned on weight-two patterns. The idea was to choose the precoder for a given PR channel which yielded the best conditional distance enumerator. Also, the distance spectrum was improved by the addition of an S-random interleaver which prevents weight-two codewords with closely spaced ones.

Fig. 3 presents simulation results for a 16-state outer RSC punctured to rate 16/17, for information-word sizes of 512 and 4096 bits, and for various precoders with EPR4 signaling and AWGN (EPR4 has the polynomial $1 + D - D^2 - D^3$). The conditional distance enumerator theory indicates that the precoder with transfer function $1/(1 + D + D^2 + D^3)$ should have the lowest floor [9], in agreement with the simulation results in the figure for both block lengths (although this is difficult to see even for the very low error rates simulated).

2.3 LDPC Schemes

Paralleling the research paths of those in the data transmission world, the study of the suitability of LDPC codes to data storage followed closely behind the PCCC and SCCC studies [10], [11]. LDPCCs, like turbo codes, attracted the attention of both researchers and practitioners in the data storage arena. These codes have turbo-like performance while offering a lower complexity decoder (although a higher complexity encoder). Further, an interleaver between the channel and encoder as in Fig. 1 is unnecessary in this case because LDPC codes already have a superior weight spectrum, and the spectral thinning [12] offered by the interleaver is therefore unnecessary. Also, the APP channel detector is usually included in the iterative decoding loop. Fig. 4 illustrates how the performance of a $(4161, 3431)$ LPDC code (rate $\simeq 5/6$) is actually slightly better than that of a rate 4/5 SCCC. (We used the irregular LDPC matrix of Mackay at http://wol.ra.phy.cam.ac.uk/mackay/.)

Because LDPCCs have large minimum distances, their block error rates are much smaller than those of the PCCC and SCCC schemes. An unfortunate consequence, however, is that, when a block is undecodable, errors come in large bursts. This is perceived by many as unacceptable. The argument made is that such a large error burst is certain to overwhelm an outer Reed-Solomon code, a necessity for the block error rate requirements of storage devices (10^{-10} or less).

2.4 The Colored Noise Situation

The work reported above is for partial response signaling and AWGN. However, as indicated in the Introduction, an actual magnetic recording channel sees colored noise due to PR equalization and media (transition) noise.

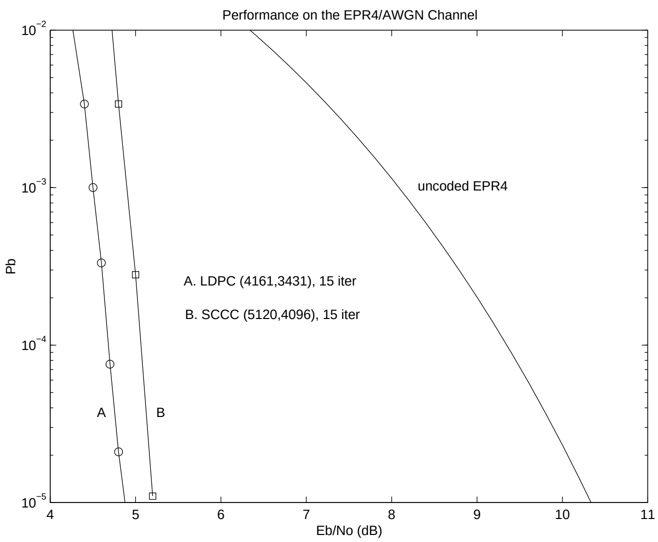

Fig. 4. Performance of the LDPC scheme (EPR4).

Research results reported for SCCCs and colored noise due to equalization only is reported in [2] and [9]. In those works, it is shown that the gains seen for the AWGN case are reduced somewhat, but they are still substantial. Also, references [2] and [9] report work on the choice of optimal code rates which, loosely speaking, arises from the fact the MRC is an ISI channel over which a balance must be struck: for a given user bit density, a lower code rate has greater inter-codeword distances, but also more ISI, and a higher code rate has smaller inter-codeword distances, but also less ISI. Research on LPDC codes together with both equalization noise and media noise was reported in [13]. Lastly, we remark that some initial work on the performance of the codes discussed in this section in the presence of thermal asperities are reported in [9] and [10].

3. TURBO CODES WITH RLL CODES

The results reported for PCCCs, SCCCs, and LDPCCs have inspired several researchers to re-examine the interface between the error control code (ECC) and the RLL code. In the "standard configuration" of Fig. 5, the soft-decision ECC decoder has to obtain reliable soft information from the constrained code decoder. It is difficult in general to perform SISO decoding for the vast majority of RLL codes since their encoders often obscure the relationship between data bits and code bits. If this SISO decoding for the constrained code is not accurate, or if the constrained code itself is not well designed, the overall constrained system can easily reflect a rate loss in excess of the nominal rate loss for the constrained code (due to error propagation) [16].

An awareness of this difficulty has motivated some recent research which has resulted in the description of several new system configurations which allow interleaved concatenated codes to be used with an arbitrary constrained code [10], [14], [2]. References

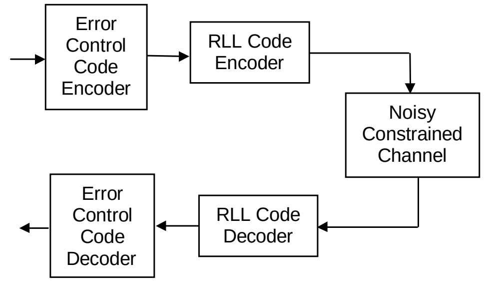

Fig. 5. Conventional RLL/ECC arrangement.

[10] and [14] study turbo codes in the "commuted configuration" of Bliss, while [2] introduces a scheme that permits use of an arbitrary $(0, k)$-constrained code with an interleaved serial concatenated system for precoded partial response systems. In both of these systems the rate loss observed in the overall system is exactly the nominal rate loss of the constrained code (assuming AWGN).

When combining SISO iterative decoders with constrained codes, it is possible in some cases to recover a portion of the nominal rate loss of the constrained code. This rate loss recovery is at the expense of higher complexity in the ECC and RLL decoders. We briefly highlight several results that pertain to such scenarios. These results are for the ideal white noise situation, where the rate loss goes as R rather than the R^2 seen in MRCs.

Consider first the commuted configuration for which the outer code is an RLL code and the inner code is a high-rate PCCC, say. For $(0, k)$ constraints, since the PCCC encoder is systematic, parity bits are periodically inserted into the $(0, k)$-constrained bit stream. In this high rate scenario, the PCCC encoder output will be $(0, k')$-constrained with $k' = k + 1 + \left\lfloor \frac{k}{n-1} \right\rfloor$ for a rate $(n-1)/n$ PCCC encoder. Therefore, for $k < n - 1$, we obtain $k' = k + 1$. The decoder for this configuration integrates the $(0, k')$ constraint into the turbo decoder via a Cartesian product, and then subsequently passes hard decisions to the $(0, k)$ code decoder. In the most straightforward case, the Cartesian product is between the state diagram of the $(0, k)$ constraint and that of the top RSC encoder. This scheme can recover some of the rate loss of the constrained code, with the amount of rate loss recovery dependent only on the constrained code efficiency and k. For high-efficiency $(0, k)$-constrained codes, coding gains up to 0.4 dB have been observed [15].

An alternative to the technique just described is to implement a SISO decoder for the RLL code in the standard configuration of Fig. 5. An exact method for implementing a SISO decoder for an arbitrary block code was first described in [16]. If this block RLL code has rate $(n-1)/n$, it is easy to show that the only $(0, k)$-constrained code with $d_{min} > 1$ is the odd single parity check (SPC) code with $d_{min} = 2$

and $k = 2n - 2$. When a SISO decoder for SPC codes is used as the constraint decoder in Fig. 5, it is capable of achieving a coding gain of over 2 dB (asymptotically for large n and E_b/N_0) in a constrained AWGN channel (no partial response). Construction of other rate $\frac{n-1}{n}$ $(0, k)$-constrained codes with $d_{min} = 1$ capable of rate recovery is possible using odd SPC codes as mother codes [17].

For constrained partial response channels, the properties of the optimal (or near-optimal) code change. In this case, the channel would be detected by an APP algorithm which may use *a priori* information derived from the $(0, k)$-constraint. Under these circumstances, systematic $(0, k)$-constrained codes are currently the best codes known in terms of rate loss recovery [17]. A systematic $(0, k)$-constrained block code of rate $k/(k + 1)$ is easily constructed by terminating every block of k unconstrained input bits with a **1**. These codes have $d_{min} = 1$, but the channel APP detector is able to make effective use of the very strong *a priori* information represented by the known positions of the **1**s in the constrained sequence. Compared with the best known constrained codes for $(0, k)$-constrained AWGN channels (the odd SPCs mentioned above), these systematic $(0, k)$-constrained block codes have two advantages. The first is that, for given codeword length n, they possess smaller k ($n - 1$ versus $2n-2$); the second is that decoding consists of simply discarding the soft information corresponding to the encoder-inserted **1**s. The efficiencies of these codes are low and this, together with their relatively large k, has made them unattractive in current systems employing hard decoders. But since these codes can be used with very low rate loss, they are good candidates for future recording systems which can tolerate the larger values of k.

References

[1] W. Ryan, "Performance of high rate turbo codes on a PR4-equalized magnetic recording channel," *Proc. 1998 Int. Conf. on Comm.*

[2] W. Ryan, "Optimal code rates for concatenated codes on a PR4-equalized magnetic recording channel," *Proc. 1999 Conf. on Inf. Sci. and Sys.* (Also, accepted for publication, *IEEE Trans. Magnetics.*)

[3] J. Wolf and G. Ungerboeck, "Trellis coding for partial response channels," *IEEE Trans. Comm.*, pp. 765-773, Aug. 1986.

[4] W. Ryan, L. McPheters, and S. McLaughlin, "Combined turbo coding and turbo equalization for PR4-equalized Lorentzian channels," *Proc. 1998 Conf. on Inf. Sci. and Sys.*

[5] T. Souvignier, A. Friedmann, M. Öberg, P. Siegel, R. Swanson, and J. Wolf, "Turbo decoding for PR4: parallel versus serial concatenation," *Proc. 1999 Int. Conf. on Comm.*

[6] L. McPheters, S. McLaughlin, and K. Narayanan, "Precoded PRML, serial concatenation, and iterative (turbo) decoding for magnetic recording," *1999 Int. Conf. on Magnetics.*

[7] W. Ryan, "Design considerations for concatenating convolutional codes with partial response channels," *Proc. 37th Allerton Conf. on Comm., Cont., and Comp.* (Sept. 1999).

[8] W. Ryan, "Concatenated Codes for Class IV Partial Response Channels," to appear, *IEEE Trans. Comm.*

[9] A. Ghrayeb and W. Ryan, "Concatenated code system design for storage channels," to appear, *JSAC Special Issue on Signal Processing for High Density Storage Channels.*

[10] J. L. Fan, *Constrained coding and soft iterative decoding for storage*, Ph.D. Dissertation, Stanford Univ., Stanford, CA, 2000.

[11] H. Song, R. Todd, and J. R. Cruz, "Low density parity check codes for magnetic recording channels," *2000 Int. Conf. on Magnetics.*

[12] L. Perez, J. Seghers, and D. Costello, "A distance spectrum interpretation of turbo codes," *IEEE Trans. Inf. Theory*, pp. 1698-1709, Nov. 1996.

[13] J. Moon, "LDPC code performance in transition noise," *ICC 2000 Workshop on Data Storage.*

[14] J. L. Fan and J. M. Cioffi, "Constrained coding techniques for soft decoders," *Proc. 1999 GlobeCom Conf.*

[15] K. D. Anim-Appiah and S. W. McLaughlin, "Constrained–input turbo codes for $(0, k)$ RLL channels," *Proc. 1999 Conf. on Information Sci. and Sys.*

[16] K. D. Anim-Appiah and S. W. McLaughlin, "Towards soft output APP decoding for nonsystematic nonlinear block codes," *Proc. 37th Allerton Conf. on Comm., Cont., and Comp.* (Sept. 1999).

[17] K. Anim-Appiah and S. McLaughlin, "Turbo Codes cascaded with high-rate block codes for $(0, k)$-constrained channels," to appear, *JSAC Special Issue on Signal Processing for High Density Storage Channels.*