

ECE 474A/574A Computer-Aided Logic Design, Fall 2006

Instructor

Susan Lysecky, slysecky@ece.arizona.edu
Office Hours: TBD
Office: ECE 320C

Teaching Assistant

Xiaoyan Wei, xwei@email.arizona.edu
Office Hours: TBD
Office: TBD

Lecture

MWF 12:00PM-12:50PM, CHVEZ 111

Textbook

(Required) Digital Design, Frank Vahid, John Wiley & Sons, ISBN 0470044373
(Optional) Logic Synthesis and Verification Algorithms, Gary Hachtel and Fabio Somenzi, Springer, ISBN 0387310045

Grading

Grading will be evaluated on an individual basis. You will not be competing with other students for your grade. If all students do well in the class, everyone will get an A. Your grade is dependent on the effort you put into the class. Letter grades will be assigned as follows: 90% and above is an A, 80% and above is a B, 70% and above is a C, 60% and above is a D, and less than 60% is an E.

The grading is based on a weighted sum as follows:

25% Final
30% Midterms (2 Midterms)
10% Homework
20% Programming Assignments
10% Term Project
5% Participation

Students enrolled in ECE 574A will have additional/different homework, lab assignments, and term project requirements.

Policies

Punctuality: Please arrive on-time to class. If you are late, try not to disrupt others and enter as quietly as possible.

Cell Phones: Please turn off you cell phone before you come to class.

Academic Dishonesty: Any academic dishonesty will not be tolerated. Unless otherwise specifically stated by your instructor or teaching assistant, all course work should be done on your own. Please consult the UA Code of Academic Integrity.

Engineering is a social discipline requiring good people skills. Study groups will enable you to get to know others in your field, while enhancing your learning. It is strongly encouraged to form study groups and review the course material together. However, you should not work on homework or lab assignment together. If you have questions on these specific problems come see the instructor or TA.

Reading: Be prepared. Read over the material before class. For the most part lecture will follow mostly the organization of the book. I will do my best to post upcoming lecture topics. Check the class webpage regularly for announcements.

Regrades: All requests for regrades must be submitted in writing within one week of the distribution of the graded material. Problems requested to be regraded will be regraded in their entirety, which could possibly result in a lower score for the requested problem.

Late Homeworks: Late homework assignment will be accepted for a maximum of two days after the due date. For each day your assignment is late, 10% of the total possible points will be deducted from your score.

Topics (including but not limited to)

- Design and implementation of sequential circuits
- Design of datapath components (register, adders, ALUs, etc.)
- Register-Transfer Level (RTL) Design
- Optimization and Tradeoffs of combinational and sequential circuits
- Heuristic Minimization of Two-Level Circuits
- Binary Decision Diagrams (BDDs)
- Multi-Level Minimization