

Susan Lysecky

Assistant Professor

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RESEARCH INTERESTS

Embedded system design, with emphasis on low-power design, sensor networks, and facilitating the design and configuration of sensor networks by non-engineers, such as scientists, agriculturalists, military personnel, home owners, etc. Research interests also include self-configuring systems, efficient architectures, and human-computer interaction.

Enhancing science and math education by developing basic intuitive building blocks students can implement a variety of systems without having any programming or electronics knowledge. Research interests also include design and implementation of intuitive devices and interfaces, developing hands-on projects to reinforce curriculum, introducing engineering as a potential and interesting field of study.

EDUCATION

Ph.D. June 2006, Computer Science, University of California, Riverside
Thesis: eBlocks: Enabling Design of Basic Embedded Systems by Novice Users.
Advisor: Dr. Frank Vahid

M.S. August 2003, Computer Science, University of California, Riverside
Thesis: Customization of Loop Caches for Embedded Systems Design.
Advisor: Dr. Frank Vahid

B.S. June 2001, Computer Science, University of California, Riverside
Graduated Cum Laude

RESEARCH AND TEACHING EXPERIENCE

Assistant Professor, 2006 - Present

Department of Electrical and Computer Engineering, University of Arizona.

- Usability of sensor networks by non-experts
- Automated application-specific configuration
- Enhancing science and math education in middle-school and high-school curriculums

Graduate Student Researcher, 2001 – 2006

Department of Computer Science and Engineering, University of California, Riverside.

- Developed eBlocks to aid non-experts to create simple monitor/control systems, specifically defined the catalog of Boolean blocks, created the corresponding physical prototypes (approximately 100 prototypes total, consisting of each of the various blocks), and created software specifying the underlying protocol and functionality of each block.
- Conducted eBlock usability testing with hundreds of users of varying experience from novice users with no programming or electronics experience, to students who have completed courses in logic design. Specifically looked at various logic block interfaces to enable the configuration of logic expressions within the network by non-expert users, the usability of state-based block interfaces, and overall system specification.
- Created an design space exploration tool that quickly aids a application developer to customize the underlying physical attributes such as voltage, frequency, baud rate, packet size, etc, to a specific

application by specifying high level goals such as lifetime, reliability, throughput, and responsiveness without having knowledge of the underlying hardware or electronics expertise.

- *US Patent Pending, Embedded Systems Building Blocks, 2004.*

Teaching/Lab Assistant, 1999 – 2004

Department of Computer Science and Engineering, University of California, Riverside.

- Teaching assistant for several upper-division digital logic design, embedded systems design, advanced embedded systems design, and capstone senior design courses.
- Developed lab assignments and course projects currently in use in two upper-division embedded systems courses taught by several faculty members and lecturers.

PATENTS

1. F. Vahid, S. Cotterell. Embedded Systems Building Blocks. US Patent Pending, 2004.

PUBLICATIONS

Journal Papers

1. A. Gordon-Ross, S. Cotterell, F. Vahid. Tiny Instruction Caches for Low Power Embedded Systems. ACM Transactions on Embedded Computing Systems (TECS), Volume 12, Number 1, pp. 120-122, January 2004.
2. R. Lysecky, S. Cotterell, F. Vahid. *A Fast On-Chip Profiler Memory using a Pipelined Binary Tree*. IEEE Transaction on Very Large Scale Integration (TVLSI), Vol. 12, No. 1, pp 120-122, January 2004.
3. F. Vahid, T. Givargis, S. Cotterell. Power Estimator Development for Embedded System Memory Tuning. Journal of Circuits, Systems and Computers (JCSC), Vol. 11, No. 5, October 2002.
4. A. Gordon-Ross, S. Cotterell, F. Vahid. Exploiting Fixed Programs in Embedded Systems: A Loop Cache Example. IEEE Computer Architecture Letters (CAL), Jan. 2002.

Conference Papers

1. S. Lysecky, F. Vahid. Automated Generation of Basic Custom Sensor-Based Embedded Computing Systems Guided by End-User Optimization Criteria. International Conference on Ubiquitous Computing (UbiComp), September 2006.
2. S. Lysecky, F. Vahid. Automated Application-Specific Tuning of Parameterized Sensor-Based Embedded System Building Blocks. International Conference on Ubiquitous Computing (UbiComp), September 2006.
3. S. Cotterell, F. Vahid. Usability of State Based Boolean eBlocks. International Conference on Human-Computer Interaction (HCII), July 2005.
4. S. Cotterell, R. Mannion, F. Vahid, H. Hsieh. eBlocks - An Enabling Technology for Basic Sensor Based Systems. IPSN Track on Sensor Platform, Tools and Design Methods for Networked Embedded Systems (SPOTS) April 2005.
5. S. Cotterell, F. Vahid. A Logic Block Enabling Logic Configuration by Non-Experts in Sensor Networks. Conference on Human Factors in Computing Systems (CHI), April 2005.
6. R. Mannion, H. Hsieh, S. Cotterell, F. Vahid. System Synthesis for Networks of Programmable Blocks. Design, Automation and Test in Europe (DATE), March 2005.
7. S. Cotterell, K. Downey, F. Vahid. Applications and Experiments with eBlocks - Electronic Blocks for Basic Sensor-Based Systems. Sensor and Ad Hoc Communications and Networks (SECON), October 2004.
8. S. Cotterell, F. Vahid, W. Najjar, H. Hsieh. First Results with eBlocks: Embedded Systems Building Blocks. CODES+ISSS Merged Conference, October 2003.
9. S. Cotterell, F. Vahid. Synthesis of Customized Loop Caches For Core-Based Embedded Systems. International Conference on Computer Aided Design (ICCAD), November 2002.

10. S. Cotterell, F. Vahid. Tuning of Loop Cache Architectures to Programs in Embedded System Design. International Symposium on System Synthesis (ISSS), October 2002.R.
11. R. Lysecky, S. Cotterell, F. Vahid. *A Fast On-Chip Profiler Memory*. IEEE/ACM 39th Design Automation Conference (DAC), June 2002.

Technical Reports

1. S. Cotterell, F. Vahid. A Logic Block Enabling Logic Configuration by Non-Experts in Sensor Networks. UC Riverside Technical Report UCR-CSE-04-09, 2004.
2. J. Villarreal, R. Lysecky, S. Cotterell, F. Vahid. *Loop Analysis of Embedded Applications*. UC Riverside Technical Report UCR-CSE-01-03, 2001.

FELLOWSHIP, AWARDS, AND HONORS

- Honorable Mention, Southern California Embedded Systems Symposium, October 2003.
- GAANN (Graduate Assistance in Areas of National Need) Fellowship from the U.S. Dept. of Education at the University of California, Riverside, 2001-2004. Fellowship includes full tuition/fees plus stipend and funding for travel, equipment, and materials for 3 years.
- Dean's Fellowship, University of California, Riverside, 2001-2002.
- Special Interest Group on Design Automation Travel Grant, ICCAD, November 2003.
- Travel Grant, CODES+ISSS October 2003,

PROFESSIONAL ACTIVITIES

- Program Committee Member, IEEE International Conference and Workshop on the Engineering of Computer Based Systems (ECBS) , 2007
- Reviewer, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2003.
- Reviewer, ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2003.
- Member, Association for Computing Machinery (ACM).
- Member, ACM Special Interest Group on Design Automation (SIGDA).
- Member, ACM Special Interest Computer-Human Interaction (SIGCHI).
- Member, Institute of Electrical and Electronics Engineers (IEEE).

PROPOSAL PREPARATION AND EQUIPMENT DONATIONS

- Assisted with proposal submitted to National Science Foundation, *Sensor Network Application Development using a CAD Methodology*, 2005.
- Assisted with proposal submitted to National Institute of Justice, *Customizable and Flexible Victim Notification Systems*, 2005.
- Assisted with proposal submitted to Intel Research, *Assistive Technologies for Proactive Health: eBlocks for In-Home Sensor Network Configuration by Everyday People*, 2005.
- Assisted with proposal submitted to Department of Defense, *Network of Embedded Sensors and Systems Research*, 2004.
- Assisted with proposal funded by National Science Foundation, *eBlocks: Embedded Systems Building Blocks*, 2003 (funded for \$360,000).
- Assisted with donation for PIC microcontrollers and programmers from Microchip, 2004 (\$1300).

ADDITIONAL EXPERIENCE

- Created solutions manual and figures for *Embedded System Design: A Unified Hardware/Software Introduction* by Frank Vahid and Tony Givargis.
- Developed lab assignments and course projects currently in use in two upper-division embedded systems courses taught by several faculty members and lecturers.
- Participated in Harvard Business Plan competition collaborating with several Harvard MBA students, 2004.
- Technical support for hardware and software used in the embedded system research lab and undergraduate and graduate embedded systems courses.
- Assisted with registration and local arrangements for CODES 2000.

PRESENTATIONS

- Presented two papers at International Conference on Ubiquitous Computing (Ubicomp), September 2006.
- Presented paper at Conference on Human Factors and Computing Systems (CHI), April 2005.
- Presented paper at Design, Automation and Test in Europe (DATE), March 2005.
- Design Automation Conference (DAC) PhD Forum, June 2004.
- Graduate Student Poster, Southern California Embedded Systems Symposium (SCESS), October 2003. Received Honorable Mention.
- Graduate Student Poster, University of California, Riverside Industry Day, November 2003.
- Presented paper at International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), October 2003.
- Presented paper at International Conference on Computer Aided Design (ICCAD), November 2002.
- Presented paper at International Symposium on System Synthesis (ISSS), October 2002.